REMARKS

Claims 1-7 were pending in the application. Claims 1 and 4-6 are rejected under 35 U.S.C. § 102(e). Claims 2-3 and 7 are rejected under 35 U.S.C. § 103(a). Claims 4-7 are canceled without prejudice or disclaimer. Applicants reserve the right to file a continuation application to capture the subject matter of canceled claims 4-7 as originally filed. Applicants have added claims 17-21, and therefore, claims 1-3 and 17-21 are pending. Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request that the Examiner reconsider and withdraw all outstanding rejections.

I. REJECTIONS UNDER 35 U.S.C. § 102(e):

The Office Action has rejected claims 1 and 4-6 as being anticipated by *Kawata et al.*, (U.S. Patent No. 6,437,394) (hereinafter "*Kawata*"). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request that the Examiner reconsider and withdraw these rejections.

For a claim to be anticipated under 35 U.S.C. § 102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. § 2131.

A. *Kawata* does not disclose the following claim limitations

Kawata does not disclose "*at least one component including a polysilicon layer having a top surface, wherein the at least one component is formed on a field oxide region configured to separate the plurality of gate stacks*" as recited in claim 1. The Examiner directs Applicants' attention to element 403 as disclosing the above-cited claim limitation. Paper No. 11, page 3. Instead, *Kawata* states:

> *403 is a gate electrode of the transistor of the peripheral circuit section* which is simultaneously generated as the control gate 205 of the flash memory cell and hence is of the same polycide structure. Meanwhile, the flash memory cell sect ion is denoted by the same reference numeral as that used in FIG. 2. Column 4, lines 49-54.

Thus, *Kawata* discloses a gate electrode of a transistor of a peripheral circuit section. This language does not disclose a *component formed on a field oxide region*. Further,

this language does not disclose a component formed on a field oxide region *configured to separate the plurality of gate stacks*. Thus, *Kawata* does not disclose all the limitations of claim 1, and thus *Kawata* does not anticipate claim 1. M.P.E.P. § 2131.

Kawata does not disclose "*a silicide on the top surface of the polysilicon layer of the at least one component*" as recited in claim 1. The Examiner directs Applicants' attention to element number 403 as disclosing the at least one component. Paper No. 11, page 3. The Examiner further directs Applicants' attention to element number 205 as disclosing the silicide on the top surface of the polysilicon layer of the at least one component. Paper No. 11, page 3. Instead, *Kawata* states:

> 205 is a control gate having a polycide structure comprised of polysilicon of the order of 150 nm doped with phosphorus and tungsten silicide of the order of 150 nm. This control gate 205 operates as a word line of the flash memory. Column 4, lines 11-15.

Thus, *Kawata* discloses a control gate having a polycide structure *doped* with phosphorus and tungsten silicide. However, the phosphorus and tungsten silicide is not on the top surface of gate electrode 403 which the Examiner asserts as disclosing the at least one component. Thus, *Kawata* does not disclose all the limitations of claim 1, and thus *Kawata* does not anticipate claim 1. M.P.E.P. § 2131.

Kawata does not disclose "*an insulating layer covering the plurality of gate stacks, the at least one component and the silicide, the insulating layer having a plurality of contact holes therein*" as recited in claim 1. The Examiner directs Applicants' attention to element 404 as disclosing the insulating layer and elements 406 and 407 as disclosing the contact holes. Paper No. 11, page 3. However, Figure 4A of *Kawata* does not disclose *an insulating layer that covers a component and the silicide on the top surface of a polysilicon layer of the component.* Thus, *Kawata* does not disclose all the limitations of claim 1, and thus *Kawata* does not anticipate claim 1. M.P.E.P. § 2131.

Kawata does not disclose "*a field oxide region located adjacent to said oxide layer*" as recited in claim 17. Further, *Kawata* does not disclose "*a component located on said field oxide region*" as recited in claim 17. Thus, *Kawata* does not

disclose all the limitations of claim 17, and thus *Kawata* does not anticipate claim 17. M.P.E.P. § 2131.

Further, *Kawata* does not disclose "*a silicide layer formed on said component*" as recited in claim 17. As stated above, *Kawata* discloses a control gate having a polycide structure *doped* with phosphorus and tungsten silicide. However, this tungsten silicide is not formed on a component located on a field oxide region. Thus, *Kawata* does not disclose all the limitations of claim 17, and thus *Kawata* does not anticipate claim 17. M.P.E.P. § 2131.

For at least the above reasons, claims 1 and 17 are not anticipated by *Kawata*. Claims 18-21 each recite combinations of features including the above combinations, and thus are not anticipated for at least the above reasons as well. Claims 18-21 recite additional features, which, in combination with the features of the claims upon which they depend, are not anticipated by *Kawata*.

For example, *Kawata* does not disclose "wherein said *silicide layer on said component prevents etching through one of said first and said second polysilicon layer*" as recited in claim 18. As stated above, *Kawata* discloses a control gate having a polycide structure doped with phosphorus and tungsten silicide. The tungsten silicide, disclosed in *Kawata*, is not formed on a component where the component is located on a field oxide region. Furthermore, the tungsten silicide, disclosed in *Kawata,* does not prevent etching through a polysilicon layer of the component. Thus, *Kawata* does not disclose all the limitations of claim 18, and thus *Kawata* does not anticipate claim 18. M.P.E.P. § 2131.

Further, *Kawata* does not disclose "wherein said *silicide layer comprises a titanium silicide*" as recited in claim 19. Further, *Kawata* does not disclose "wherein said *silicide layer comprises a cobalt silicide*" as recited in claim 20. Further, *Kawata* does not disclose "wherein said *component comprises a resistor*" as recited in claim 21. Thus, *Kawata* does not disclose all the limitations of claims 19-21, and thus *Kawata* does not anticipate claims 19-21. M.P.E.P. § 2131.

B. **Rejection of claims 4-6 as product-by-process claims**

The Examiner asserts that claims 4-6 are product-by-process claims and that the patentability of claims 4-6 are determined by the patentability of the final product and not by the process. Paper No. 11, page 4. The Examiner makes the implied assertion that *Kawata* discloses the flash memory device claimed in claim 1 and that since claims 4-6 are product-by-process claims directed to the product claimed in claim 1 that *Kawata* necessarily discloses the limitations of claims 4-6. However, claims 4-6 are not product-by-process claims such as illustrated in *In re Thorpe*. *In re Thorpe*, 227 U.S.P.Q. 964, 695 (Fed. Cir. 1985).[1] Further, assuming *arguendo* that claims 4-6 are product-by-process claims, these claims would still be patentable since the product as claimed in claim 1 is different from the product disclosed in *Kawata*. *In re Thorpe,* at 966. Therefore, the Examiner's rejection of claims 4-6 for being product-by-process claims is improper. However, Applicants have cancelled claims 4-6 without prejudice or disclaimer, and thus the rejection of claims 4-6 is moot.

C. **Conclusion regarding 35 U.S.C. § 102 rejections**

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation is found within *Kawata*, and thus claims 1 and 17-21 are not anticipated by *Kawata*.

It is noted that words are italicized only for emphasis. Words that are italicized are not meant to imply that only those limitations are not disclosed in the cited prior art.

II. REJECTIONS UNDER 35 U.S.C. § 103(a):

The Office Action has rejected claims 2-3 as being unpatentable over *Kawata* in view of *Nariani* (U.S. Patent No. 5,470,775) (hereinafter "*Nariani*"). The Office Action has further rejected claim 7 under 35 U.S.C. § 103 as being unpatentable over *Kawata* in view of *Diorio et al.* (U.S. Patent No. 5,990,512) (hereinafter "*Diorio*").

[1] An example of a product-by-process cited in *In re Thorpe* is claim 44 which recites "The product of the process of claim 1."

Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

A. **The Examiner has not provided any motivation for combining *Kawata* with *Nariani***

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. § 2142. The motivation or suggestion to combine references must come from one of three possible sources: the nature of the problem to be solved, the teaching of the prior art or the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 47 U.S.P.Q.2d. 1453, 1458 (Fed. Cir. 1998). The showings must be clear and particular. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

In order to reject under 35 U.S.C. § 103, therefore, the Examiner must provide a proper motivation for combining or modifying the references. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457-1458 (Fed. Cir. 1998); M.P.E.P. § 2142. The Examiner's motivation for modifying *Kawata* to have a silicide that includes a titanium silicide or a cobalt silicide is "*so as to use it as an etch stop layer.*" Paper No. 11, page 5. However, the Examiner has not offered any evidence to support this alleged motivation.

The Examiner has not established a *prima facie* case of obviousness. The Examiner has not provided any suggestion or motivation in either *Kawata* or *Nariani*, or in their combination, or in the knowledge of those ordinarily skilled in the art, to combine the teaching of decreasing the word line resistance without being accompanied by an increase in chip area in a non-volatile semiconductor memory

device, as taught in *Kawata*, with the teaching of the fabrication of a capacitor, as taught in *Nariani*.

Kawata states:

> To provide a non-volatile semiconductor memory device in which the word line resistance can be decreased in resistance without being accompanied by increase in chip area, and a manufacturing method for the non-volatile semi conductor memory device. In a non-volatile semiconductor memory device having a floating gate (203 of FIG. 2) and a control gate (205 of FIG. 2), a contact groove (407 of FIG. 4a) extending in the direction of a word line (102 of FIG. 1) is provided on an interlayer insulating film (404 of FIG. 4a) formed as an upper layer of the control gate, and an electrically conductive member of, for example, tungsten, is embedded in the contact groove to establish electrical connection between the wiring metal (409 of FIG. 4d) formed as an upper layer of the interlayer insulating film and the control gate with a large contact area. Abstract.

Thus, *Kawata* teaches a non-volatile semiconductor memory device in which a word line is subject to lining (or backing-up) a wiring as an overlaying layer to reduce the resistance without being accompanied by an increase in chip area.

Nariani states:

> A method produces a capacitor. On a substrate, a first polysilicon layer is formed over an insulating region. A metal-silicide layer is formed on top of the first polysilicon layer. A dielectric layer is formed on top of the metal-silicide layer. A second polysilicon layer is formed on top of the dielectric layer. The second polysilicon layer and the dielectric layer are etched to form a top electrode and dielectric region. The metal-silicide layer and the first polysilicon layer are etched to form a bottom electrode. Abstract.

> The present invention has several advantages over the prior art processes. For example, the present invention provides for a method which is simple, practical and fully compatible with current VLSI processes using polycide transistor gates. The performance characteristics of the integrated circuit components are unperturbed. The resulting capacitor has superior linearity and low current leakage. Further, the additional steps which are additional to conventional processing may be performed at relatively low processing temperatures (e.g., less than 850 degrees Centigrade), preserving reliability of the VLSI circuitry. Column 2, lines 1-16.

Thus, *Nariani* teaches a method for fabricating a capacitor with superior linearity and lower current leakage than the prior art.

The Examiner has not shown why the teaching of a non-volatile semiconductor memory device in which a word line is subjected to lining a wiring as an overlaying layer to reduce the resistance without being accompanied by an increase in chip area, as taught in *Kawata*, should be combined with the teaching of a method of fabricating a capacitor, as taught in *Nariani*, from either the nature of the problem to be solved, the teaching in the prior art or the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 42 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). The Examiner must submit **objective** evidence and not rely on his own subjective opinion for combining *Kawata*, which teaches a non-volatile semiconductor memory device in which a word line is subjected to lining a wiring as an overlaying layer to reduce the resistance without being accompanied by an increase in chip area with *Nariani*, which teaches a method for fabricating a capacitor. *In re Lee*, U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Moreover, the Examiner has not shown why *Kawata* should be modified to have a silicide that includes either a titanium silicide or a cobalt silicide from either the nature of the problem to be solved, the teaching in the prior art or the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). Further, the Examine has not shown why *Kawata* should be modified to use a silicide as an etch stop layer from either the nature of the problem to be solved, the teaching in the prior art or the knowledge of persons of ordinary skill in the art. *Id.* Neither *Kawata* nor *Nariani* teach the use of a silicide as an etch stop layer. Therefore, one of ordinary skill in the art would not be motivated to modify any devices taught by the references to include a silicide as an etch stop layer.

The Examiner must submit **objective evidence** and not rely on his own subject opinion in support of modifying *Kawata* to have a silicide that includes either a titanium silicide or a cobalt silicide. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Further, the Examiner must submit **objective evidence** and not rely on his own subjective opinion in support of modifying *Kawata* to have a silicide used as an

etch stop layer. *Id.* Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2-3 and 19-20.

B. *Kawata* and *Nariani*, taken singly or in combination, do not teach or suggest the following limitations

Kawata and *Nariani*, taken singly or in combination, also do not teach or suggest "*wherein the silicide further includes a titanium silicide*" as recited in claim 2 and similarly in claim 19. *Kawata* and *Nariani*, taken singly or in combination, do not teach or suggest "*wherein the silicide further includes a cobalt silicide*" as recited in claim 3 and similarly in claim 20. As stated above, the Examiner directs Applicants' attention to element 205 in *Kawata* as teaching a silicide on the top surface of the polysilicon layer of a component. Paper No. 11, page 3. The Examiner further directs Applicants' attention to column 2, lines 59-67 of *Nariani* as teaching a silicide layer that may be either a titanium silicide or a cobalt silicide. Paper No. 11, page 5. As stated above, *Kawata* does not teach a component where the component is formed on a field oxide region. Further, neither *Kawata* nor *Nariani*, taken singly or in combination, teach or suggest a silicide on a component formed on a field oxide region . Instead, *Nariani* states:

> After insulating layer 25 is formed, a layer of gate oxide 35 is placed (i.e. grown or deposited) on exposed portions of the substrate. A layer of polysilicon 26 is deposited over the layer of gate oxide 35 and insulating layer 25. For example, the deposition may be a chemical vapor deposition (CVD). The polysilicon is doped, for example, with n-type atoms at approximately 10^{20} atoms per cubic centimeter. The doping may be performed using $POCl_3$. Alternately, an implant of Phosphorus or Arsenic atoms may be used. Alternately, an in situ doped polysilicon may be deposited. A metalsilicide layer 27 is formed on top of polysilicon layer 26, for example by chemical vapor deposition at approximately 400 degrees Centigrade or by sputtering at approximately 200 degrees Centigrade. For example, the metal-silicide may be Tungsten-silicide. The metal used for metal-silicide layer 27 may alternately consist of, for example, Titanium (Ti) Molybdenum (Mo), Chromium (Cr), Nickel (Ni), Cobalt (Co), or Tantalum (Ta). Column 2, lines 50-67.

Thus, *Nariani* teaches depositing polysilicon layer 26 over the layer of gate oxide 35 and insulating layer 25. *Nariani* further teaches forming a middle silicide layer 27 on

top of polysilicon layer 26. This middle silicide layer is not placed on top of a component formed on a field oxide region. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2-3 and 19-20. M.P.E.P. § 2143.

C. **Examiner's reliance on *Sinclair & Carroll Co., Inc. v. Interchemical Corp.* is misplaced**

The Examiner notes in his rejection to claims 2-3 that a "selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair & Carroll Co., Inc. v. Interchemical Corp.*, 325 U.S. 327, 65 U.S.P.Q. 297 (1945)." Paper No. 11, page 5. Applicants note that *Sinclair & Carroll*, upon which the Examiner relies, precedes *Graham vs. John Deere Co.*, 383 U.S. 1, 148 U.S.P.Q. 459 (1966). Thus, to the extent that *Sinclair & Carroll Co.* anticipates the factual analysis mandated in *Graham*, they are merely cumulative of *Graham*. Conversely, to the extent that as contrary to the factual inquiry mandated by *Graham*, it must be deemed overruled by *Graham*.

Furthermore, if the Examiner cites this case to suggest that the Examiner does not have a burden of providing objective evidence for modifying *Kawata* to have a silicide layer that may be either a titanium silicide or a cobalt silicide, the Examiner is mistaken. As stated above, the Examiner must submit **objective evidence** and not rely on his own subjective opinion for modifying *Kawata* to have a silicide that includes either a titanium silicide or a cobalt silicide. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Furthermore, Applicants assert that the Examiner's use of *Sinclair & Carroll Co.* is misplaced. In *Sinclair & Carroll Co.*, the U.S. Supreme Court determined that Gessler's patent on a particular ink was invalid since the ink was already known. *Sinclair & Carroll Co.* at 335. However, Applicants are not attempting to procure a patent on either titanium silicide or cobalt silicide. Hence the citing of *Sinclair & Carroll Co.* by the Examiner is misplaced.

D. The Examiner has not provided any motivation for combining *Kawata* with *Diorio*

As stated above, a *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. § 2142. The motivation or suggestion to combine references must come from one of three possible sources: the nature of the problem to be solved, the teaching of the prior art and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 47 U.S.P.Q.2d. 1453, 1458 (Fed. Cir. 1998). The showings must be clear and particular. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

In order to reject under 35 U.S.C. § 103, therefore, the Examiner must provide a proper motivation for combining or modifying the references. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457-1458 (Fed. Cir. 1998); M.P.E.P. § 2142. The Examiner's motivation for modifying *Kawata to* have a component located on a field oxide layer is to provide "*a channel stop to adjust the transistor's threshold voltage.*" Paper No. 11, page 6.

The Examiner has not established a *prima facie* case of obviousness. The Examiner has not provided any suggestion or motivation in either *Kawata* or *Diorio*, or in their combination, or in the knowledge of those ordinarily skilled in the art, to combine the teaching of decreasing the word line resistance without being accompanied by an increase in chip area in a non-volatile semiconductor memory device, as taught in *Kawata*, with the teaching of a silicon analog memory cell which can be written and erased as well as written and read simultaneously on a single device, as taught in *Diorio*.

As stated above, *Kawata* teaches a non-volatile semiconductor memory device in which a word line is subject to lining (or backing-up) a wiring as an overlaying layer to reduce the resistance without being accompanied by an increase in chip area. *Diorio* states:

> Accordingly, there is a need for an improved silicon analog memory cell which can be written and erased, which can be written and read simultaneously, and which can be realized in a single device. Column 4, lines 7-10.

Thus, *Diorio* teaches a silicon analog memory cell which can be written and erased as well as written and read simultaneously on a single device.

The Examiner has not shown why the teaching of a non-volatile semiconductor memory device in which a word line is subjected to lining a wiring as an overlaying layer to reduce the resistance without being accompanied by an increase in chip area, as taught in *Kawata*, should be combined with the teaching of a silicon analog memory cell which can be written and erased as well as written and read simultaneously, from either the nature of the problem to be solved, the teaching in the prior art or the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 42 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). The Examiner must submit **objective evidence** and not rely on his own subjective opinion for combining *Kawata*, which teaches a non-volatile semiconductor memory device in which a word line is subjected to lining a wiring as an overlaying layer to reduce the resistance without being accompanied by an increase in chip area with *Diorio*, which teaches a silicon analog memory cell which can be written and erased as well as written and read simultaneously. *In re Lee*, U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Moreover, the Examiner has not shown why *Kawata* should be modified to have a field oxide region where a component is located on the field oxide region, from either the nature of the problem to be solved, the teaching in the prior art or the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). Further, the Examine has not shown why *Kawata* should be modified to have a channel stop to adjust the transistor's threshold voltage from either the nature of the problem to be solved, the teaching in the prior art or the knowledge

of persons of ordinary skill in the art. *Id.* Neither *Kawata* nor *Diorio* teach adjustment of the transistor's threshold voltage, as required by Applicants' claim.

The Examiner must submit **objective evidence** and not rely on his own subject opinion in support of modifying *Kawata* to have a field oxide region where a component is located on the field oxide region. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Further, the Examiner must submit **objective evidence** and not rely on his own subjective opinion in support of modifying *Kawata* to have a channel stop to adjust the transistor's threshold voltage. *Id.* Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1, 7 and 17.

E. Rejection of claim 7 under 35 U.S.C. § 103(a) is moot

As stated above, the Office Action has rejected claim 7 under 35 U.S.C. § 103(a) as being unpatentable over *Kawata* in view of *Diorio*. Applicants have cancelled claim 7 without prejudice or disclaimer, and therefore the rejection of claim 7 is moot.

F. Claims 1 and 17 are patentable over *Kawata* in view of *Diorio*

Kawata and *Diorio*, taken singly or in combination, do not teach or suggest "wherein the at *least one component is formed on a field oxide region configured to separate the plurality of gate stacks*" as recited in claim 1 and similarly in claim 17. The Examiner directs Applicants' attention to element 24 as teaching "a component" and element 26 as teaching a field oxide region. Instead, *Diorio* states:

> (1) *Electrons tunnel from the floating gate 24, through the 350 A gate oxide 26, to the tunneling implant 28.* A relatively high positive voltage applied to the tunneling implant 28 provides the oxide E-field required for tunneling. To prevent reverse-bias pn-junction breakdown at the tunneling implant 28, the tunneling implant 28 is disposed in a lightly doped n^- well 30. Because tunneling removes electrons from the floating gate, from the control gate's (20) perspective tunneling reduces the transistor's threshold voltage V_t. Column 10, lines 5-13.

Thus, *Diorio* teaches electrons tunnel from the floating gate 24 through gate oxide 26 to the tunneling implant 28. The Examiner has not explained why floating gate 24 is not a component. Furthermore, gate oxide 26 is not used to separate a plurality of

gate stacks. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1 and 17. M.P.E.P. § 2143.

Kawata and *Diorio*, taken singly or in combination, do not teach or suggest "*a field oxide region located adjacent to said oxide layer*" as recited in claim 17. As stated above, *Diorio* teaches electrons tunnel from the floating gate 24 through gate oxide 26 to the tunneling implant 28. Referring to Figure 6B in *Diorio*, gate oxide 26 is not adjacent to an oxide layer where a gate stack is formed on the oxide layer. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 17. M.P.E.P. § 2143.

G. Conclusion regarding 35 U.S.C. § 103 rejections

As a result of the foregoing, Applicants respectfully assert that since there are numerous claim limitations not taught or suggested in the cited prior art, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2-3, 7 and 17 in view of the cited prior art.

It is noted that words are italicized only for emphasis. Words that are italicized are not meant to imply that only those limitations are not taught or suggested in the cited prior art.

III. CONCLUSION

As a result of the foregoing, it is asserted by Applicants that claims 1-3 and 17-21 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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